

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Priority Application Serial No. 10/459,064
Priority Filing Date June 10, 2003
Inventor Leonard Forbes
Assignee Micron Technology, Inc.
Priority Group Art Unit 2818
Priority Examiner V. Nguyen
Attorney's Docket No. MI22-2481
Title: Computer Systems, Processes For Turning A SRAM Cell Off, and Processes For
Writing A SRAM Cell and Processes for Reading Data From A SRAM Cell

EL979949726

INFORMATION DISCLOSURE STATEMENT
PURSUANT TO 37 C.F.R. §§ 1.56, 1.97 AND 1.98

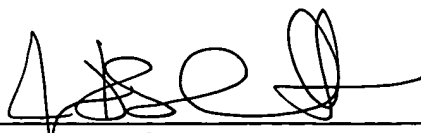
In compliance with 37 C.F.R. §§ 1.56, 1.97 and 1.98, your attention is directed to the United States patents and other references listed on the attached Form PTO-1449. No admission is made regarding whether all the submitted references are prior art.

The listed references were cited by, or submitted to, the Office in the parent, co-pending application of the above-identified application. The above-identified application is a divisional application of co-pending application Serial No. 10/459,064, filed July 10, 2003. Such prior disclosure is sufficient for the above-identified application as far as copies of the references are concerned. 37 C.F.R. § 1.98(d) and MPEP § 609(2).

Citation of these references is respectfully requested.

Respectfully submitted,

Dated: 4/6/04

By: 
James D. Shaurette
Reg. No. 39,833

Form PTO-1449		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. MI22-2481	PRIORITY SERIAL NO. 10/459,064	
LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)				APPLICANT Leonard Forbes		
				PRIORITY FILING DATE July 10, 2003	PRIORITY GROUP 2818	
U.S. PATENT DOCUMENTS						
*Examiner Initial	Document Number	Date	Name	Class	Subclasses	Filing Date If Appropriate
	AA	6,128,216	10/03/00	Noble, Jr. et al.		
	AB	5,825,687	10/20/98	Yin		
	AC	6,287,913 B1	09/11/01	Agnello et al.		
	AD	5,754,468	05/19/98	Hobson		
	AE	6,104,045	08/15/00	Forbes et al.		
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	AG	6,342,718 B1	01/29/02	Noble		
	AH	6,194,759 B1	02/2001	Sano et al.		
	AI	6,459,113 B1	10/01/02	Moribara et al.		
	AJ	2002/0028550 A1	03/07/02	Moribara et al.		
	AK	6,011,726	01/04/00	Batson et al.		
FOREIGN PATENT DOCUMENTS						
	Document Number	Date	Country	Class	Subclass	Abstract
						Yes No
	AL	10-335488	12/1998	Japan		
	AM	JP02001308298 A	11/02/01	Japan		X
	AN					
	AO					
	AP					
OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)						
	AR	Lage et al., "Advanced SRAM technology - the rate between 4T and 6T cells," Abstract (Web address - http://pluto.ei.org),				
		Technical Digest - Proceedings of the 1996 IEEE International Electron Devices Meeting Dec. 8-11, 1996.				
	AS	Noda et al., "A 1.9- μm^2 Loadless CMOS Four-Transistor SRAM Cell in a 0.18- μm Logic Technology", 1998,				
		ULSI Device Development Laboratories, NEC Corporation, Japan, 5 pages.				
	AT					
EXAMINER		DATE CONSIDERED				
<p>*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.</p>						

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U.S. PATENT DOCUMENTS						
*Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA	6,184,588	2/2001	Kim et al.		
	AB	5,774,392	6/1998	Kraus et al.		
	AC	6,212,102	4/2001	Georgakos et al.		
	AD	6,265,266	7/2001	Dejenfelt et al.		
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	AK	6,090,648	7/18/2000	Reedy et al.		
FOREIGN PATENT DOCUMENTS						
	Document Number	Date	Country	Class	Subclass	Abstract
						Yes No
	AL					
	AM					
	AN					
	AO					
	AP					
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